

APPLICATION NOTE

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Measurement of Stored Charge in High Speed Diodes

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Use of stored charge to characterize the switching speed of a diode simplifies testing and improves measurement reproducibility.

As faster diodes are developed to meet the requirements of modern high speed logic circuits the problems of measuring and specifying the switching speed of the diodes are increased. Measurement of the reverse recovery time requires expensive sampling oscilloscopes with difficult measurement and calibration procedures, while the nature of the reverse recovery time measurement itself results in poor measurement reproducibility. An alternate method for characterizing the switching speed of a diode by direct measurement of the stored charge minimizes these problems. By observing a few simple precautions in the construction and use of the test circuit a direct measurement of the stored charge in a diode can be made on inexpensive equipment with a high degree of reproducibility.

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GENERAL DESCRIPTION

Forward current in a semiconductor diode is carried by minority carriers (holes or electrons) which are injected by the junction into the adjacent semiconductor material. Under equilibrium conditions a total minority carrier charge, Q_{tot} , will exist in the diode at a given value of forward current, I_F . The value of Q_{tot} will depend principally on four factors: (1) the value of I_F , (2) the impurity distribution in the vicinity of the junction, (3) the width of the semiconductor material, and (4) the lifetime of the minority carriers in the semiconductor material. To a first approximation Q_{tot} will be directly proportional to the forward current, I_F . The lifetime of the semiconductor material can be controlled in manufacture over a wide range by techniques such as the introduction of a controlled amount of gold which acts as a recombination center for the minority carriers.

When a forward biased diode is subjected to a reverse voltage step a reverse current will flow for a short time as a result of the stored charge within the diode. A typical waveform for a diode subjected to a large reverse voltage is shown in Figure 1. The time required for the diode to recover its blocking condition will depend on the quantity of charge stored, the rate at which the charge is removed by recombination within the diode, and by the magnitude of the current flowing in the external circuit. The percentage of the total charge, Q_{tot} , which is recovered will increase as the reverse current drive is increased, but can not exceed a certain maximum value determined by the structure of the diode. For a wide base alloy diode the percentage of the total charge which is recovered can not exceed 50%, while for some types of snap-off diodes the percentage of the total charge recovered can be as high as 95%.

When a diode biased at zero volts and zero current is subjected to a reverse voltage step a reverse current will flow as a result of the charging of the junction barrier capacitance, the stray capacitance and the jig capacitance. The capacitance charging current is shown by the lower amplitude curve in Figure 1. To a first approximation the capacitive charge is independent of the initial forward bias current since the initial and final circuit voltages across the diode are the same.

The stored charge, Q_S , can be defined as the recovered minority carrier charge measured under circuit conditions which are chosen to maximize the recovered charge. The capacitive component of measured charge can be eliminated by taking the difference between the total recovered charge at two different values of forward bias current.

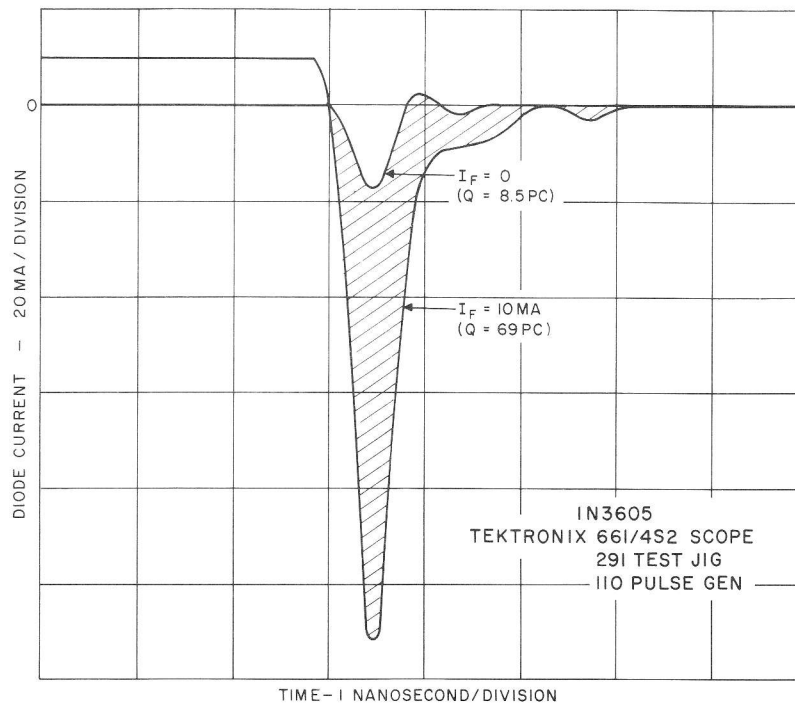


Figure 1. Reverse Recovery Characteristics of Silicon Planar Epitaxial Diode Measured Under High Reverse Current Conditions

OSCILLOSCOPE MEASUREMENT OF Q_S

The stored charge of a high speed diode can be measured with a sampling oscilloscope and a X-Y recorder. The diode is placed in a suitable test jig which may be similar to those used for reverse recovery time measurements. In some cases it may be necessary to reduce the effective source and load impedance of the test jig to satisfy the requirements for a high reverse current drive. The pulse generator should have a rise time which is as short as possible. Using a X-Y recorder connected to the output of the sampling oscilloscope the reverse recovery characteristic of the diode under test is recorded both at zero bias voltage and at the required forward bias current. Figure 1 illustrates a typical recording of this type. Current and time calibration marks are also made on the same recording. The area under the two curves is then obtained using a planimeter or by counting squares, and the difference between the two areas is taken to obtain Q_S . This corresponds to the shaded area shown in Figure 1 and is equal to $69 \text{ pc} - 8.5 \text{ pc} = 60.5 \text{ pc}$.

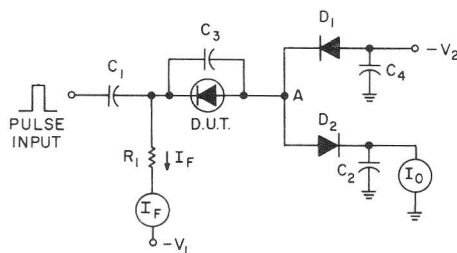


Figure 2. Basic Stored Charge Measurement Circuit

DIRECT MEASUREMENT OF Q_S .

Stored charge can be measured directly without the need for elaborate circuits and complex integration techniques. The basic circuit for direct measurement of stored charge is shown in Figure 2. The diode under test (DUT) is forward biased by the current flowing through the bias current meter I_F , R_1 , and D_1 . A positive pulse at a known frequency is coupled from the pulse generator through C_1 to the DUT. This pulse reverse biases the DUT and the charge stored in the DUT flows through D_2 into the integrating capacitor C_2 and the output meter I_O . With a forward current I_F flowing the current through the output meter, I_2 , will be proportional to the stored charge, the capacitive charge, and the leakage current;

$$I_2 = fQ_S + fV_P C'_{avg} + ft_P I_r \quad (1)$$

where f is the pulse frequency, V_P is the pulse amplitude, C'_{avg} is the average capacitance (DUT plus jig) over the voltage range from V_F to $V_F - V_P$, V_F is the forward voltage of the DUT at a forward current of I_F , t_P is the pulse width, and I_r is the reverse current of the DUT measured at a reverse voltage equal to V_P . If the voltage across the DUT is set to zero by adjusting V_1 , the current through the output meter, I_1 , will be proportional to the capacitive charge and the leakage current;

$$I_1 = fV_P C_{avg} + ft_P I_r \quad (2)$$

where C_{avg} is the average capacitance (DUT plus jig) over the voltage range from 0 to $-V_P$.

The stored charge is obtained by taking the difference between Equation 1 and Equation 2 and dividing by the frequency, f . The stored charge is defined by the equation;

$$Q_S = \frac{I_2 - I_1}{f} \quad (3)$$

Note that there is a component of capacitive charge contained in the definition of Equation 3 since C'_{avg} and C_{avg} are not equal as a result of the dependence of the junction barrier capacitance on voltage. This means that it is possible for a diode with no minority carrier stored to have a finite measureable stored charge as defined above. This compromise in the exact definition of stored charge is the more practical choice since it simplifies the measurement of Q_S and relates Q_S to common circuit usage. The voltage excursions to which diodes are subjected in most switching applications are generally greater than the forward voltage drop of the diode, hence the particular capacitive component can be considered inseparable from Q_S .

Since the value of Q_S as defined above involves the difference between two bias conditions it reduces the dependence of the measurement on the pulse voltage, the stray capacitance and the reverse current of the DUT and thus provides a more significant parameter for characterizing the diode. Effects of leakage current, junction capacitance, pulse amplitude, and pulse width can be considered separately by the designer when estimating the performance of a diode in a given circuit.

CIRCUIT PRECAUTIONS

Circuit precautions must be observed when building and using the test circuit of Figure 2 particularly when making measurements on high speed diodes. The time constant $R_1 C_1$ should be large compared to the pulse width to maintain constant voltage across the DUT during the pulse. The output impedance of the pulse generator and the rise time of the pulse should both be as low as possible to ensure maximum recovery of the available stored charge from the DUT. A sharp "front corner" is required on the pulse, otherwise the DUT will be reverse biased for an appreciable time before the voltage at point A has become sufficiently positive to bias D_2 into conduction with the result that a portion of the available stored charge will be lost through recombination within the diode. To minimize measurement errors occurring from this cause the 1% to 50% rise time of the pulse is specified rather than the conventional 10% to 90% rise

time. The pulse should also have a top which is as flat as possible with a minimum of overshoot or ringing.

Diode D_1 passes the forward current of the DUT between pulses. It should have a low reverse leakage current and a much smaller value of stored charge than the DUT. A regulator (avalanche) diode which has a low dynamic impedance in the breakdown region and a low capacitance below the breakdown region can be used for D_1 if the DUT has a very low value of stored charge. During the pulse, diode D_2 passes the stored charge of the DUT to the capacitor C_2 and the meter. The large pulse of current that flows through D_2 makes it necessary that the turn on time and the forward voltage drop of D_2 both be as small as practical. To prevent loss of measured charge through D_2 at the end of the pulse, the reverse recovery time of D_2 should be much shorter than the minimum pulse width.

Capacitor C_2 provides a low impedance path for the stored charge which flows from the DUT through D_2 during the pulse. This capacitor should be large enough so that there is no appreciable voltage drop across it during the pulse. The current meter used should be of a type which has a low input impedance so that there is no appreciable voltage drop across it when making a stored charge measurement.

Capacitor C_3 , which includes the capacitance of the test jig, serves to forward bias D_2 at the beginning of the pulse so that the full charge of the DUT can flow through D_2 rather than being partly lost in charging the capacitance between point A and ground. The size of C_3 will be adequate if a small current flows through the output meter when the DUT is removed. Capacitor C_3 should not be made too large since it will then serve to reduce the rise time of the pulse generator.

To ensure recovery of the maximum amount of stored charge from the DUT, the inductance of all the circuit loops should be kept to a minimum by the use of low inductance components and by careful circuit layout.

Voltage source V_2 should be adjusted so that the voltage at point A is maintained constant at each test condition. If this was not done, the voltage at point A would change as the forward current through the DUT was changed owing to the finite resistance of D_1 . Thus, the amount of charge required by the capacitance between point A and ground would change as the forward current through the DUT was changed and this would result in a corresponding error in the Q_S reading. Voltage source V_2 is normally adjusted so that the voltage at point A is -0.6 volts with respect to ground. Slight

changes in the voltage at point A can be used to compensate for minor variations in the parameters of the test circuit so as to achieve better uniformity in stored charge measurements of very high speed diodes.

The measurement method as described is somewhat tedious in that it involves taking measurements at two bias conditions, adjusting V_2 to maintain the voltage at point A constant, and taking the difference between the two output current readings. However, an operational amplifier can be used to sense the voltage at point A and adjust the voltage at V_2 to maintain the voltage at point A constant. Also, the bias current to the DUT can be chopped between the two required values and the output current can be synchronously demodulated to provide a direct indication of Q_S . In addition to the advantage of providing a direct reading of Q_S the chopper technique has the additional advantage of eliminating the need for a zero adjustment on the output meter. Incorporation of these techniques in the basic stored charge test circuit has permitted the measurement of Q_S to be made on a simple "plug in and read" basis.

TEST SPECIFICATIONS

In most cases the forward bias current and the pulse amplitude are sufficient to describe Q_S measurement conditions. However, to ensure reproducible measurements on high speed diodes it is frequently desirable to provide additional information including; pulse width, pulse generator output impedance, pulse rise time (1% to 50%), Q_S of D_1 , forward recovery time of D_2 , high current forward voltage of D_2 , and Q_S of D_2 .

Typical test specifications for commercial Q_S measurement equipment are;
 $f = 100$ kc, $V_P = 5$ volts, pulse generator impedance = 10 ohms, $t_P = 50$ nanoseconds, pulse rise time = 0.4 nanoseconds, and $I_F = 0.1, 1, 10$ milliamperes.

TEST RESULTS

Measurements of Q_S have been performed on a wide variety of diode types ranging from ultra fast gallium arsenide sampling diodes to very slow silicon rectifier diodes. For high speed silicon computer diodes measured on independently calibrated Q_S test equipment the reproducibility of Q_S readings ranges was found to range from 1% to 5%. This contrasts with a reproducibility of 5% to 40% for reverse recovery time measured on the same type of diodes. Reproducibility of measurements on the same Q_S equipment is generally better than 1%, while the short term stability of readings is generally better than 0.01%. Stored charge measured by use of the previously described sampling

scope technique generally agrees with the direct measurement of stored charge to within 2%. For example, the measured Q_S for the diode shown in Figure 1 was 62 picocoulombs as compared with the value of 60.5 picocoulombs obtained by integration of the waveform.

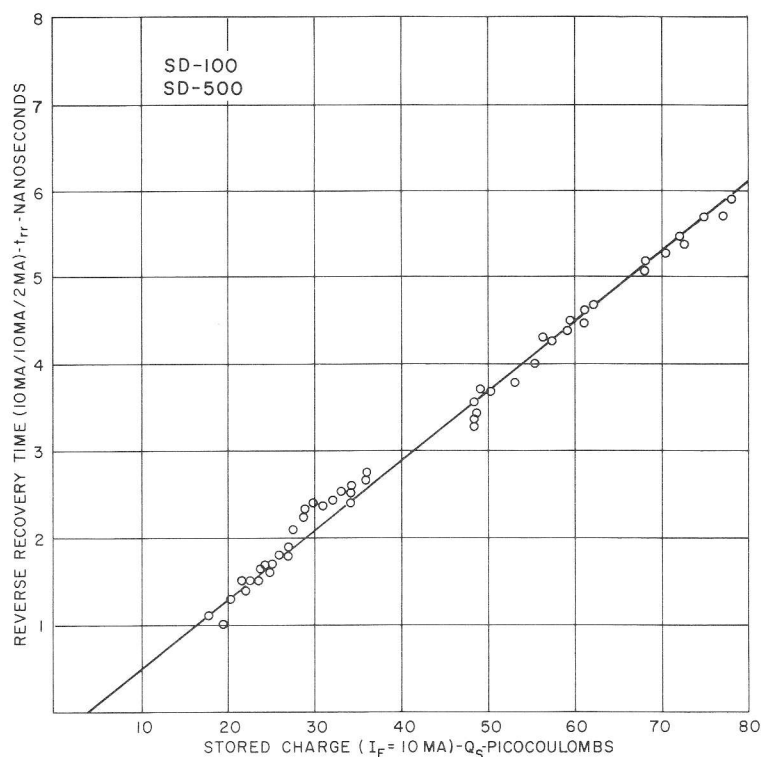


Figure 3. Correlation Plot Between Stored Charge and Reverse Recovery Time

Correlation between Q_S and reverse recovery time, t_{rr} , is usually within the uncertainty of the reverse recovery time reading. A correlation plot of Q_S vs t_{rr} for high speed silicon planar epitaxial diodes is shown in Figure 3. To illustrate that the major part of the deviation from exact correlation is due to the t_{rr} measurement rather than the Q_S measurement a correlation plot of t_{rr} for two different test conditions is shown in Figure 4 for the same group of diodes. The assumption is frequently made that measurement of t_{rr} at one particular condition will ensure the performance of a diode in a switching circuit operating under different conditions. Figure 4 indicates that there may be a large uncertainty in such a relationship and that the percent-

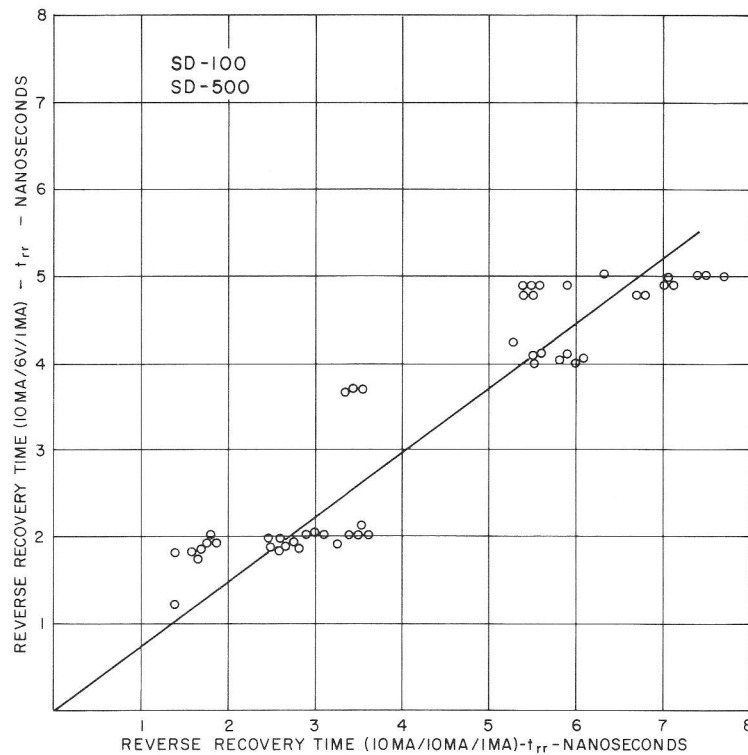


Figure 4. Correlation Plot Between Reverse Recovery Time Measured at Two Different Test Conditions

age uncertainty is larger for higher speed diodes. Much of the dispersion in the data of Figure 4 is a direct result of the nature of the reverse recovery time measurement itself. Small discontinuities or mismatches in the diode test fixture will produce large distortions in the diode current waveform in the region where t_{rr} is measured. These distortions in the current waveform result in significant differences in measured t_{rr} values for the same diode in different jigs even when great care is taken in the construction of the jigs to ensure uniformity and good performance. In the measurement of Q_S , on the other hand, this problem is avoided since the reverse recovery waveform is integrated and the effects of small distortions in the waveform are minimized.

The variation of Q_S with forward current is shown in Figure 5 for a typical silicon planar epitaxial diode. The nonlinearity at low current levels is due primarily to the small contribution of junction capacitance to the Q_S reading. The nonlinearity is less pronounced for diodes with a higher value of Q_S .

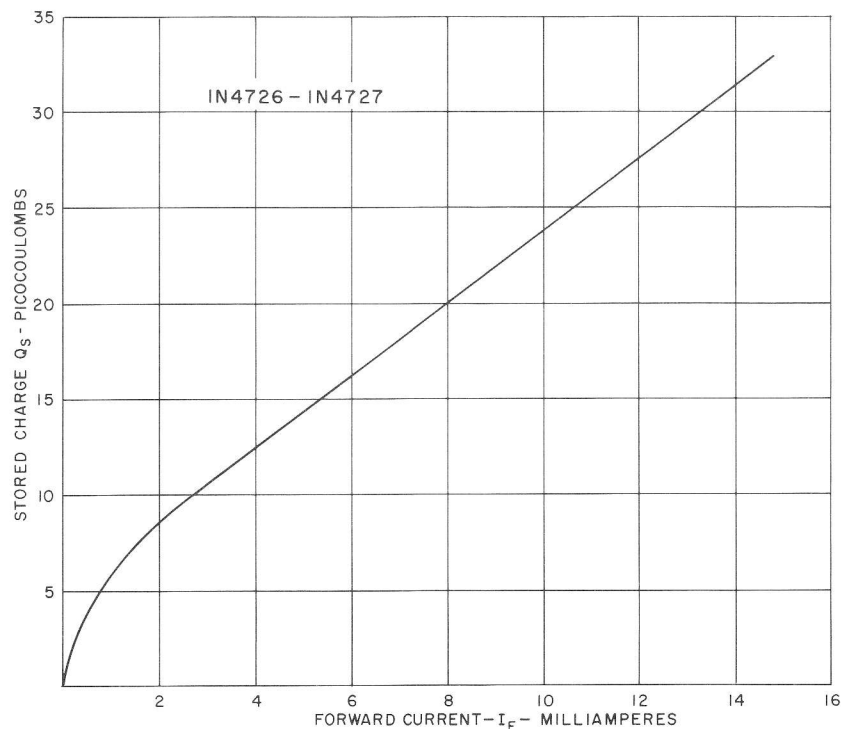


Figure 5. Variation of Stored Charge with Forward Current for a Silicon Planar Epitaxial Diode

Figure 6 gives the correlation between Q_S and t_{rr} measured at three different test conditions for a group of silicon planar epitaxial diodes.

SUMMARY

- (1) Stored charge provides a single unambiguous figure of merit for a switching diode which can be specified without an elaborate set of test conditions and test jig construction details.
- (2) The test circuit for measurement of stored charge is simple and relatively inexpensive. A direct meter readout is possible even with high speed diodes, and the use of an expensive sampling scope is avoided.
- (3) Reproducibility of stored charge measurements is better than the reproducibility of reverse recovery time measurements.
- (4) For faster circuits which are charge sensitive rather than waveform sensitive, stored charge is a parameter which can be used directly in circuit analysis.

- (5) Comparative readings of stored charge can be made on ultra-fast diodes which can not be measured on the faster sampling scopes.
- (6) The test method described conforms to method 4061 of MIL-STD-750 and to the JEDEC proposed standard for direct measurement of diode stored charge.

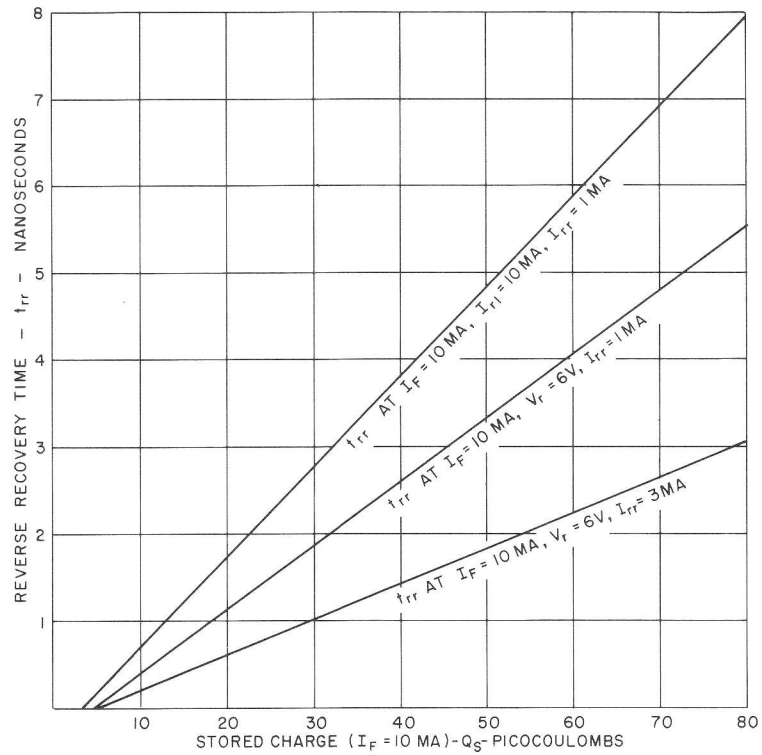


Figure 6. Variation of Reverse Recovery Time at Various Test Conditions with Stored Charge for Silicon Planar Epitaxial Diodes

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